THYTRONIC

PRO N

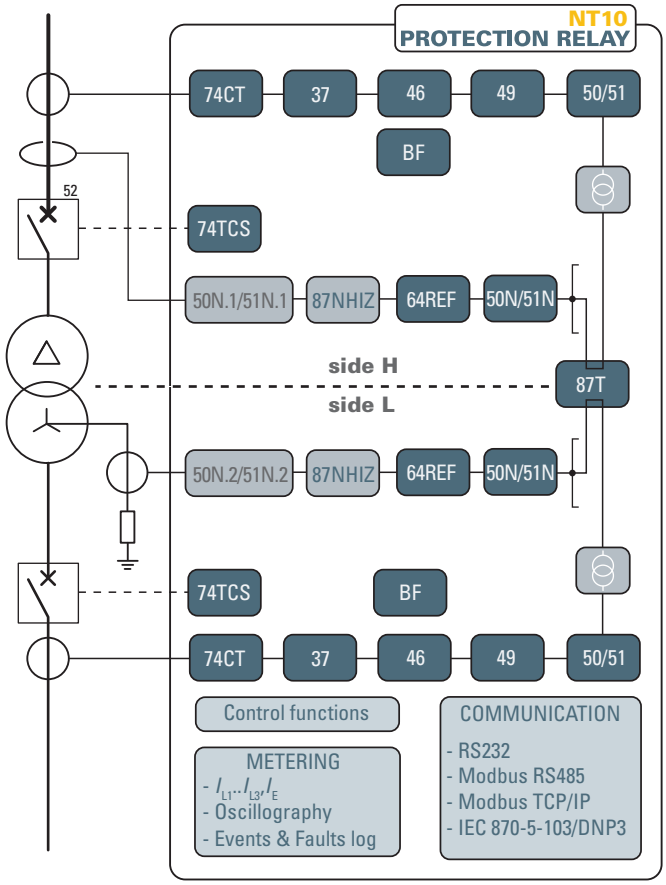
NT10

TRANSFORMER PROTECTION RELAY

RESTRAINED DIFFERENTIAL
FOR TWO WINDINGS TRANSFORMERS WITH OVERCURRENT ELEMENTS AND THERMAL IMAGE

— Application

The NT10 relay is suitable for two windings MV, LV power transformers.
The adjustment of amplitude and phase current differential protection can be achieved through internal compensation (sw) or through the use of external adapters.



- Protective & control functions

37	Phase undercurrent
46	Negative-sequence overcurrent
49	Thermal image
50/51	Phase overcurrent
50N/51N	Residual overcurrent
64REF	Biased restricted differential ground fault
I2/I1	Phase interruption under low-load condition
87NHIZ	High impedance restricted ground fault
87T	Double slope biased differential for two windings transformers
BF	Breaker Failure
74CT	CTs monitoring
74TCS	Trip circuit supervision

— Firmware updating

The use of flash memory units allows on-site firmware updating.

— Construction

According to the hardware configurations, the protection relay can be shipped in various case styles depending on the required mounting options (flush, projecting mounting, rack or with separate operator panel).

— Modular design

In order to extend I/O capability, the NT10 hardware can be customized through external auxiliary modules:

- MRI - Output relays and LEDs
- MID16 - Binary inputs
- MCI - 4...20 mA converter
- MPT - Pt100 probe inputs.

— Measuring inputs

- Three phase current inputs for the H side
- Three phase current inputs for the L side
- Two residual current inputs for the H side or the L side

For all inputs the rated currents are independently selectable to 1 A or 5 A through DIP-switches.

— Binary inputs

Two binary inputs are available with programmable active state (active-ON/active-OFF) and programmable timer (active to OFF/ON or ON/OFF transitions).

— Output relays

Six output relays are available (two changeover, three make and one break contacts); each relay may be individually programmed as normal state (normally energized, de-energized or pulse) and reset mode (manual or automatic).
A programmable timer is provided for each relay (minimum pulse width). The user may program the function of each relay in accordance with a matrix (tripping matrix) structure.

— Metering

NT10 provides metering values for phase and residual currents, making them available for reading on a display or to communication interfaces.
Input signals are sampled 16 times per period and the RMS value of the fundamental component is measured using the DFT (Discrete Fourier Transform) algorithm and digital filtering.
With DFT the RMS value of 2nd and 5th harmonic of differential phase current are also measured.
On the base of the direct measurements, the calculated residual current, the stabilization currents, the sequence currents, the thermal image, the differential phase currents, minimum-peak-fixed-rolling demand, mean-minimum-maximum absolute phase currents are processed.
The measured signals can be displayed with reference to nominal values or directly expressed in amperes.

— Differential protection for two-windings transformer

In order to correct any polarity reversals or phase cyclic sequence, equal amplitude and phase currents on the two sides of differential protection and to clearing the zero sequence component, the relay performs the compensation of amplitude, polarity, to phase and cyclic sequence and zero sequence currents.
In the case of internal compensation, the compensation is calculated by the relay as follows:

- Calculation of the rated currents of the transformer sides from rated power and voltages
- Calculation of the difference (mismatching) between the CT primary rated current and rated current of the sides of the transformer
- Choosing the side of the transformer (RefSide) that compensations in current amplitude are related.

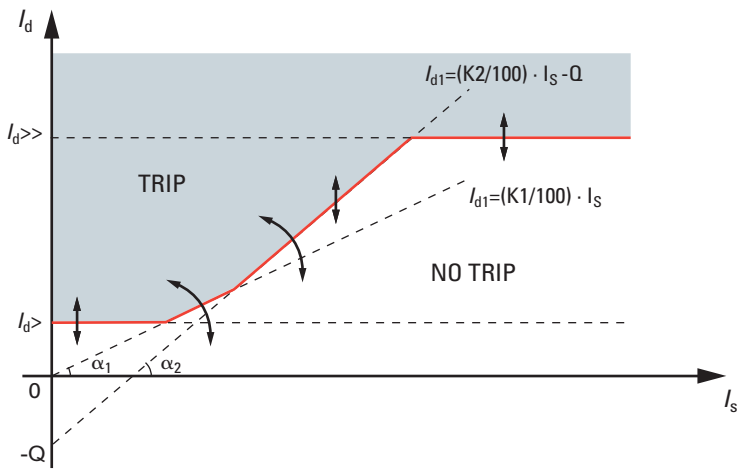
The polarity compensation (Polarity matching) allows us to consider each input current with its angular phase or with opposite phase angle, thus allowing the correction of any reverse polarity sw amperometric due to link errors.
The phase compensation and cyclic sequence and zero sequence allows the sw correction of the currents displacement on the sides of the transformer due to the vectorial group, any phases reversal cyclic sequence and the elimination of any zero sequence components that may occur on some side due to the windings connecting and its ground connection when ground fault outside the zone of differential protection arises.

— Two set point profiles (A,B)

Two independent groups of settings are provided. Switching from profiles may be operated by means of MMI, binary input and communication.

— MMI (Man Machine Interface)

The user interface comprises a membrane keyboard, a backlight LCD alphanumeric display and eight LEDs.
The green ON LED indicates auxiliary power supply and self diagnostics, two LEDs are dedicated to the Start and Trip (yellow for Start, red for Trip) and five red LEDs are user assignable.



— Control and monitoring

Several predefined functions are implemented:

- Circuit Breaker commands and diagnostic.
- Activation of two set point profiles.
- Phase CTs monitoring (74CT).
- Logic selectivity.
- Cold load pickup (CLP) with block or setting change.
- Trip circuit supervision (74TCS).
- Harmonic restraint.
- Remote tripping.

User defined logic may be customized according to IEC 61131-3 standard protocol (PLC).

Circuit Breaker commands and diagnostic

Several diagnostic, monitoring and control functions are provided:

- Health thresholds can be set; when the accumulated duty (ΣI or ΣI^2t), the number of operations or the opening time exceeds the threshold an alarm is activated.
- Breaker failure (BF); breaker status is monitored by means 52a-52b and/or through line current measurements.
- Trip Circuit Supervision (74TCS).
- Breaker control; opening and closing commands can be carried out locally or remotely.

Cold Load Pickup (CLP)

The Cold Load Pickup feature can operate in two following modes:

- Each protective element can be blocked for a adjustable time.
- Each threshold can be increased for a programmable time.

It is triggered by the circuit breaker closing.

Harmonic restraint

To prevent unwanted tripping of the protective functions on transformer inrush current, the protective elements can be blocked when the ratio between the second and/or the fifth harmonic differential currents and the relative fundamental current is larger than a user programmable threshold.
The function can also be programmed to switch an output relay so as to cause a blocking protection relays lacking in second harmonic restraint.

Logic selectivity

With the aim of providing a fast selective protection system some protective functions may be blocked (pilot wire accelerated logic). To guarantee maximum fail-safety, the relay performs a run time monitoring for pilot wire continuity and pilot wire shorting. Exactly the output blocking circuit periodically produces a pulse, having a small enough width in order to be ignored as an effective blocking signal by the input blocking circuit of the upwards protection, but suitable to prove the continuity of the pilot wire. Furthermore a permanent activation (or better, with a duration longer than a preset time) of the blocking signal is identified, as a warning for a possible short circuit in the pilot wire or in the output circuit of the downstream protection.
The logic selectivity function can be realized through any combination of binary inputs, output relays and/or committed pilot wires circuits.

— Self diagnostics

All hardware and software functions are repeatedly checked and any anomalies reported via display messages, communication interfaces, LEDs and output relays.
Anomalies may refer to:

- Hw faults (auxiliary power supply, output relay coil interruptions, MMI board...).
- Sw faults (boot and run time tests for data base, EEPROM memory checksum failure, data BUS,...).
- Pilot wire faults (break or short in the wire).
- Circuit breaker faults.

— Communication

Multiple communication interfaces are implemented:

- One RS232 local communication front-end interface for communication with ThySetter setup software
- Two back-end interfaces for communication with remote monitoring and control systems by:
  - RS485 port - ModBus® RTU, IEC 60870-5-103 or DNP3 protocol,
  - Ethernet port (RJ45 or optical fiber) - ModBus/TCP protocol.

— Blocking input/outputs

One output blocking circuit and one input blocking circuit are provided.
The output blocking circuits of one or several Pro_N relays, shunted together, must be connected to the input blocking circuit of the protection relay, which is installed upwards in the electric plant. The output circuit works as a simple contact, whose condition is detected by the input circuit of the upwards protection relay. For long distances, when high insulation and high EMC immunity is essential, a suitable pilot wire to fiber optic converter (BFO) is available.

— Event storage

Several useful data are stored for diagnostic purpose; the events are stored into a non volatile memory.
They are graded from the newest to the older after the "Events reading" command (ThySetter) is issued:

- Sequence of Event Recorder (SER)
  The event recorder runs continuously capturing in circular mode the last three hundred events upon trigger of binary input/output.
- Sequence of Fault Recorder (SFR)
  The fault recorder runs continuously capturing in circular mode the last twenty faults upon trigger of binary input/output and/or element pickup (start-trip).
- Trip counters

— Digital Fault Recorder (Oscillography)

Upon trigger of tripping/starting of each function or external signals, the relay records in COMTRADE format:

- Oscillography with instantaneous values for transient analysis.
- RMS values for long time periods analysis.
- Logic states (binary inputs and output relays).

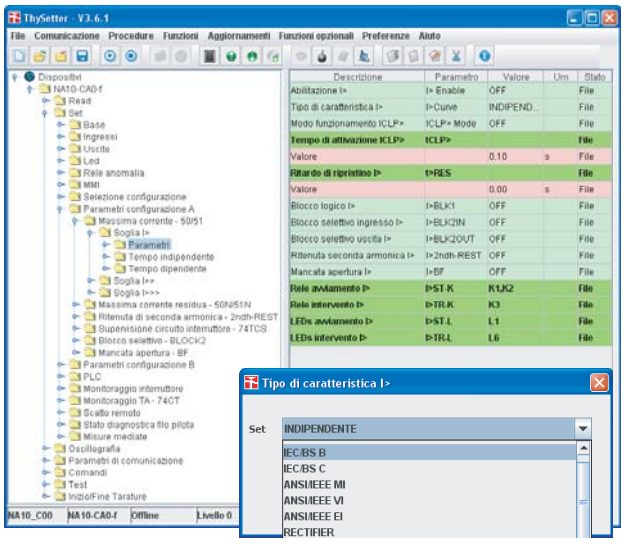
— Programming and settings

All relay programming and adjustment operations may be performed through MMI (Keyboard and display) or using a Personal Computer with the aid of the ThySetter software.
The same PC setup software is required to set, monitor and configure all Pro_N devices.
Full access to the available data is provided:

- Read status and measures.
- Read/edit settings (on-line or off-line edit).

Two session level (User or Administrator) with password for sensible data access are provided.

ThySetter



SPECIFICATIONS

GENERAL

— Mechanical data

Mounting:	flush, projecting, rack or separated operator panel
Mass (flush mounting case)	2.0 kg

— Insulation tests

Reference standards	EN 60255-5
High voltage test 50Hz	2 kV 60 s
Impulse voltage withstand (1.2/50 µs)	5 kV
Insulation resistance	>100 MΩ

— Voltage dip and interruption

Reference standards	EN 61000-4-29

— EMC tests for interference immunity

1 MHz damped oscillatory wave	EN 60255-22-1	1 kV-2.5 kV
Electrostatic discharge	EN 60255-22-2	8 kV
Fast transient burst (5/50 ns)	EN 60255-22-4	4 kV
Conducted radio-frequency fields	EN 60255-22-6	10 V
Radiated radio-frequency fields	EN 60255-4-3	10 V/m
High energy pulse	EN 61000-4-5	2 kV
Magnetic field 50 Hz	EN 61000-4-8	1 kA/m
Damped oscillatory wave	EN 61000-4-12	2.5 kV
Ring wave	EN 61000-4-12	2 kV
Conducted common mode (0...150 kHz)	EN 61000-4-16	10 V

— Emission

Reference standards	EN 61000-6-4 (ex EN 50081-2)
Conducted emission 0.15...30 MHz	Class A
Radiated emission 30...1000 MHz	Class A

— Climatic tests

Reference standards	IEC 60068-x, ENEL R CLI 01, CEI 50

— Mechanical tests

Reference standards	EN 60255-21-1, 21-2, 21-3

— Safety requirements

Reference standards	EN 61010-1
Pollution degree	3
Reference voltage	250 V
Overvoltage	III
Pulse voltage	5 kV
Reference standards	EN 60529
Protection degree:	
• Front side	IP52
• Rear side, connection terminals	IP20

— Environmental conditions

Ambient temperature	-25...+70 °C
Storage temperature	-40...+85 °C
Relative humidity	10...95 %
Atmospheric pressure	70...110 kPa

— Certifications

Product standard for measuring relays	EN 50263
CE conformity	
• EMC Directive	2004/108/EC
• Low Voltage Directive	2006/95/EC
Type tests	IEC 60255-6

COMMUNICATION INTERFACES

Local PC RS232	19200 bps
Network:	
• RS485	1200...57600 bps
• Ethernet 100BaseT	100 Mbps
Protocol	ModBus® RTU/IEC 60870-5-103/DNP3, TCP/IP,

INPUT CIRCUITS

— Auxiliary power supply Uaux

Nominal value (range)	24...48 Vac/dc, 115...230 Vac/110...220 Vdc
Operative range (each one of the above nominal values)	19...60 Vac/dc
	85...265 Vac/75...300 Vdc
Power consumption:	
• Maximum (energized relays, Ethernet TX)	10 W (20 VA)
• Maximum (energized relays, Ethernet FX)	15 W (25 VA)

— Phase current inputs - sides H and L

Nominal current I_n	1 A or 5 A selectable by DIP Switches
Permanent overload	25 A
Thermal overload (1s)	500 A
Rated consumption (for any phase)	≤ 0.002 VA (I_n = 1 A)
	≤ 0.04 VA (I_n = 5 A)

— Residual current inputs - IE1 and IE2

Nominal current I_{En}	1 A or 5 A selectable by DIP Switch
Permanent overload	25 A
Thermal overload (1s)	500 A
Rated consumption	≤ 0.006 VA (I_{En} = 1 A), ≤ 0.012 VA (I_{En} = 5 A)

— Binary inputs

Quantity	2
Type	dry inputs
Max permissible voltage	19...265 Vac/19...300 Vdc
Max consumption, energized	
3 mA	

— Block input (Logic selectivity)

Quantity	1
Type	polarized wet input (powered by internal isolated supply)
Max consumption, energized	5 mA

OUTPUT CIRCUITS

— Output relays K1...K6

Quantity	6
• Type of contacts K1, K2	changeover (SPDT, type C)
• Type of contacts K3, K4, K5	make (SPST-NO, type A)
• Type of contacts K6	break (SPST-NC, type B)
Nominal current	8 A
Nominal voltage/max switching voltage	250 Vac/400 Vac
Breaking capacity:	
• Direct current (L/R = 40 ms)	50 W
• Alternating current (λ = 0,4)	1250 VA
Make	1000 W/VA
Short duration current (0,5 s)	30 A

— Block output (Logic selectivity)

Quantity	1
Type	optocoupler

— LEDs

Quantity	8
• ON/fail (green)	1
• Start (yellow)	1
• Trip (red)	1
• Allocatable (red)	5

GENERAL SETTINGS

— Rated values

Relay nominal frequency (f_n)	50, 60 Hz
Relay phase nominal current - sides H and L (I_{nH}, I_{nL})	1 A, 5 A
Phase CT nominal primary current (I_{npH}, I_{npL})	1 A...50 kA
Relay residual nominal current (I_{En1}, I_{En2})	1 A, 5 A
Residual CT nominal primary current (I_{En1p}, I_{En2p})	1 A...50 kA
Primary nominal current choised as reference (I_{nref}) [1]	- A
Side reference for compensation (*Refside*) [1]	- (H)
Current matching type (*Matchtype*)	
	INTERNAL/EXTERNAL

Note 1 - Calculated by the relay

— Transformer data

Transformer nominal power (S_{nt})	0.01...1000 MVA
Transformer nominal voltage side H (V_{ntH})	0.200...500 kV
Transformer nominal current side H (I_{ntH}) [1]	-
Transformer mismatching factor side H (m_H) [1]	-
Transformer base current side H (I_{BH}) [1]	- I_{nH}
Transformer grounding side H (G_{ndH})	In/Out
Transformer connection side H (C_{onnH})	Y/D/Z
Transformer vector group side H ($V_{ectGroupH}$)	0
Transformer nominal voltage side L (V_{ntL})	0.200...500 kV
Transformer nominal current side L (I_{ntL}) [1]	-
Transformer mismatching factor side L (m_L) [1]	-
Transformer base current side L (I_{BL}) [1]	- I_{nL}
Transformer grounding side L (G_{ndL})	In/Out
Transformer connection side L (C_{onnL})	y/d/z
Transformer vector group side L ($V_{ectGroupL}$)	0-1-2...11

Note 1 - Calculated by the relay

— Binary input timers

ON delay time (IN1 t_{ON}, IN2 t_{ON},...IN5 t_{ON})	0.00...100.0 s
OFF delay time (IN1 t_{OFF}, IN2 t_{OFF},...IN5 t_{OFF})	0.00...100.0 s
Logic	Active-ON/Active-OFF

— Relay output timers

Minimum pulse width (t_{TR})	0.000...0.500 s

— Input sequence

Phase current sequence side H (*I-SequenceH*)
IL1-IL2-IL3, IL1-IL3-IL2....
Phase current sequence side L (*I-SequenceL*)
IL1-IL2-IL3, IL1-IL3-IL2....

— Polarity

C09-C10 (IL1H)	NORMAL/REVERSE
C11-C12 (IL21H)	NORMAL/REVERSE
C...- C... (I..)	NORMAL/REVERSE
C07-C08 (IE2)	NORMAL/REVERSE

PROTECTIVE FUNCTIONS

— Thermal protection with RTD thermometric probes - 26

Alarm
- Alarm threshold θ_{ALx} (x=1...8) 0...200 °C
- Operating time $t_{\theta ALx}$ (x=1...8) 0....100 s

Trip
- Trip threshold $\theta_{>x}$ (x=1...8) 0...200 °C
- Operating time $t_{\theta>x}$ (x=1...8) 0....100 s

Note: The element becomes available when the MPT module is enabled and connected to Thybus

— Undercurrent - 37 side H

I_H< Element
- 37 Operating logic (*Logic*37$_H$) AND/OR
- 37 First threshold definite time ($I_{H<def}$) 0.10...1.00 I_{nH}
- I_H< Operating time ($t_{IH<def}$) 0.04...200 s

— Undercurrent - 37 side L

I_L< Element
- 37 Operating logic (*Logic*37$_L$) AND/OR
- 37 First threshold definite time ($I_{L<def}$) 0.10...1.00 I_{nL}
- I_L< Operating time ($t_{IL<def}$) 0.04...200 s

— Negative sequence - 46 side H

I_{2H}> Element
- I_{2H}> Curve type DEFINITE
  IEC/BS A, B, C - ANSI/IEEE MI, VI, EI, I^2t or EM
- I_{2HCLP}> Activation time ($t_{2HCLP>}$) 0.00...100.0 s
- I_{2H}> Reset time delay ($t_{2H>RES}$) 0.00...100.0 s

Definite time
- 46 First threshold definite time ($I_{2H>def}$) 0.100...10.00 I_{nH}
- $I_{2H>def}$ within CLP ($I_{2HCLP>def}$) 0.100...10.00 I_{nH}
- $I_{2H>def}$ Operating time ($t_{2H>def}$) 0.03...200 s

Inverse time
- 46 First threshold inverse time ($I_{2H>inv}$) 0.100...10.00 I_{nH}
- $I_{2H>inv}$ within CLP ($I_{2HCLP>inv}$) 0.100...10.00 I_{nH}
- $I_{2H>inv}$ Operating time ($t_{2H>inv}$) 0.02...60.0 s

I_{2H}>> Element
- I_{2HCLP}>> Activation time ($t_{2HCLP>>}$) 0.00...100.0 s
- I_{2H}>> Reset time delay ($t_{2H>>RES}$) 0.00...100.0 s

Definite time
- 46 Second threshold definite time ($I_{2H>>def}$) 0.100...40.00 I_{nH}
- $I_{2H>>def}$ within CLP ($I_{2HCLP>>def}$) 0.100...40.00 I_{nH}
- $I_{2H>>def}$ Operating time ($t_{2H>>def}$) 0.03...10.00 s

— Negative sequence - 46 side L

I_{2L}> Element
- I_{2L}> Curve type DEFINITE
  IEC/BS A, B, C - ANSI/IEEE MI, VI, EI, I^2t or EM
- I_{2LCLP}> Activation time ($t_{2LCLP>}$) 0.00...100.0 s
- I_{2L}> Reset time delay ($t_{2L>RES}$) 0.00...100.0 s

Definite time
- 46 First threshold definite time ($I_{2L>def}$) 0.100...10.00 I_{nL}
- $I_{2L>def}$ within CLP ($I_{2LCLP>def}$) 0.100...10.00 I_{nL}
- $I_{2L>def}$ Operating time ($t_{2L>def}$) 0.03...200 s

Inverse time
- 46 First threshold inverse time ($I_{2L>inv}$) 0.100...10.00 I_{nL}
- $I_{2L>inv}$ within CLP ($I_{2LCLP>inv}$) 0.100...10.00 I_{nL}
- $I_{2L>inv}$ Operating time ($t_{2L>inv}$) 0.02...60.0 s

I_{2L}>> Element
- I_{2LCLP}>> Activation time ($t_{2LCLP>>}$) 0.00...100.0 s
- I_{2L}>> Reset time delay ($t_{2L>>RES}$) 0.00...100.0 s

Definite time
- 46 Second threshold definite time ($I_{2L>>def}$) 0.100...40.00 I_{nL}
- $I_{2L>>def}$ within CLP ($I_{2LCLP>>def}$) 0.100...40.00 I_{nL}
- $I_{2L>>def}$ Operating time ($t_{2L>>def}$) 0.03...10.00 s

— Negative sequence current / positive sequence current ratio - I_2/I_1 side H

(I_{2H}/I_{1H})> Element
- $(I_{2H}/I_{1H})_{CLP}$> Activation time ($t_{21HCLP>}$) 0.00...100.0 s

Definite time
- I_{2H}/I_{1H} First threshold definite time ($I_{21H>def}$) 0.10...1.00
- $(I_{2H}/I_{1H})_{>def}$ within CLP ($I_{21HCLP>}$) 0.10...1.00
- (I_{2H}/I_{1H})> Operating time ($t_{21H>def}$) 0.04...15000 s

— Negative sequence current / positive sequence current ratio - I_2/I_1 side L

(I_{2L}/I_{1L})> Element
- $(I_{2L}/I_{1L})_{CLP}$> Activation time ($t_{21LCLP>}$) 0.00...100.0 s

Definite time
- I_{2L}/I_{1L} First threshold definite time ($I_{21L>def}$) 0.10...1.00
- $(I_{2L}/I_{1L})_{>def}$ within CLP ($I_{21LCLP>}$) 0.10...1.00
- (I_{2H}/I_{1H})> Operating time ($t_{21H>def}$) 0.04...15000 s

— Thermal image - 49 side H

Common configuration:
- Initial thermal image $\Delta\theta_{INH}$ (D_{thINH}) 0.0...1.0 $\Delta\theta_{BH}$
- Reduction factor at inrush (K_{INRH}) 1.0...3.0
- Thermal time constant τ (T_H) 1...200 min
- Dth_{CLPH} Activation time ($t_{DthCLPH}$) 0.00...100.0 s

DtH_{AL1H} Element
- 49 First alarm threshold $\Delta\theta_{AL1H}$ (D_{thAL1H}) 0.3...1.0 $\Delta\theta_{BH}$

DtH_{AL2H} Element
- 49 Second alarm threshold $\Delta\theta_{AL2H}$ (D_{thAL2H}) 0.5...1.2 $\Delta\theta_{BH}$

Dth> Element
- 49 Trip threshold $\Delta\theta_H$ ($D_{thH>}$) 1.100...1.300 $\Delta\theta_{BH}$

— Thermal image - 49 side L

Common configuration:
- Initial thermal image $\Delta\theta_{INL}$ (D_{thINL}) 0.0...1.0 $\Delta\theta_{BL}$
- Reduction factor at inrush (K_{INRL}) 1.0...3.0
- Thermal time constant τ (T_L) 1...200 min
- Dth_{CLPH} Activation time ($t_{DthCLPL}$) 0.00...100.0 s

DtH_{AL1L} Element
- 49 First alarm threshold $\Delta\theta_{AL1L}$ (D_{thAL1L}) 0.3...1.0 $\Delta\theta_{BL}$

DtH_{AL2L} Element
- 49 Second alarm threshold $\Delta\theta_{AL2L}$ (D_{thAL2L}) 0.5...1.2 $\Delta\theta_{BL}$

Dth> Element
- 49 Trip threshold $\Delta\theta_L$ ($D_{thL>}$) 1.100...1.300 $\Delta\theta_{BL}$

— Phase overcurrent - 50/51 side H

I_H> Element

- I_H> Curve type (I_H>Curve) DEFINITE
  IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, RECTIFIER, I^2t or EM
- I_{HCLP}> Activation time ($t_{HCLP>}$) 0.00...100.0 s
- I_H> Reset time delay ($t_{H>RES}$) 0.00...100.0 s

Definite time

- 50/51 First threshold definite time ($I_{H>def}$) 0.100...40.0 I_{nH}
- $I_{H>def}$ within CLP ($I_{HCLP>def}$) 0.100...40.0 I_{nH}
- $I_{H>def}$ Operating time ($t_{H>def}$) 0.04...200 s

Inverse time

- 50/51 First threshold inverse timee ($I_{H>inv}$) 0.100...20.00 I_{nH}
- $I_{H>inv}$ within CLP ($I_{HCLP>inv}$) 0.100...20.00 I_{nH}
- $I_{H>inv}$ Operating time ($t_{H>inv}$) 0.02...60.0 s

I_H>> Element

- I_H>> Type characteristic (I_H>>Curve) DEFINITE, I^2t
- I_{HCLP}>> Activation time ($t_{HCLP>>}$) 0.00...100.0 s
- I_H>> Reset time delay ($t_{H>>RES}$) 0.00...100.0 s

Definite time

- 50/51 Second threshold definite time ($I_{H>>def}$) 0.100...40.0 I_{nH}
- $I_{H>>def}$ within CLP ($I_{HCLP>>def}$) 0.100...40.0 I_{nH}
- $I_{H>>def}$ Operating time ($t_{H>>def}$) 0.03...10.00 s

Inverse time

- 50/51 Second threshold inverse time ($I_{H>>inv}$) 0.100...20.00 I_{nH}
- $I_{H>>inv}$ within CLP ($I_{HCLP>>inv}$) 0.100...20.00 I_{nH}
- $I_{H>>inv}$ Operating time ($t_{H>>inv}$) 0.02...10.00 s

I_H>>> Element

- I_{HCLP}>>> Activation time ($t_{HCLP>>>}$) 0.00...100.0 s
- I_H>>> Reset time delay ($t_{H>>>RES}$) 0.00...100.0 s

Definite time

- 50/51 Third threshold definite time ($I_{H>>>def}$) 0.100...40.0 I_{nH}
- $I_{H>>>def}$ within CLP ($I_{HCLP>>>def}$) 0.100...40.0 I_{nH}
- $I_{H>>>def}$ Operating time ($t_{H>>>def}$) 0.03...10.00 s

— Phase overcurrent - 50/51 side L

I_L> Element

- I_L> Curve type (I_L>Curve) DEFINITE
  IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, RECTIFIER, I^2t or EM
- I_{LCLP}> Activation time ($t_{LCLP>}$) 0.00...100.0 s
- I_L> Reset time delay ($t_{L>RES}$) 0.00...100.0 s

Definite time

- 50/51 First threshold definite time ($I_{L>def}$) 0.100...40.0 I_{nL}
- $I_{HL>def}$ within CLP ($I_{LCLP>def}$) 0.100...40.0 I_{nL}
- $I_{L>def}$ Operating time ($t_{L>def}$) 0.04...200 s

Inverse time

- 50/51 First threshold inverse time ($I_{L>inv}$) 0.100...20.00 I_{nL}
- $I_{L>inv}$ within CLP ($I_{HCLP>inv}$) 0.100...20.00 I_{nL}
- $I_{L>inv}$ Operating time ($t_{L>inv}$) 0.02...60.0 s

I_L>> Element

- I_L>> Type characteristic (I_L>>Curve) DEFINITE, I^2t
- I_{HLCLP}>> Activation time ($t_{LCLP>>}$) 0.00...100.0 s
- I_L>> Reset time delay ($t_{L>>RES}$) 0.00...100.0 s

Definite time

- 50/51 Second threshold definite time ($I_{L>>def}$) 0.100...40.0 I_{nL}
- $I_{L>>def}$ within CLP ($I_{LCLP>>def}$) 0.100...40.0 I_{nL}
- $I_{L>>def}$ Operating time ($t_{L>>def}$) 0.03...10.00 s

Inverse time

- 50/51 Second threshold inverse time ($I_{L>>inv}$) 0.100...20.00 I_{nL}
- $I_{L>>inv}$ within CLP ($I_{LCLP>>inv}$) 0.100...20.00 I_{nL}
- $I_{L>>inv}$ Operating time ($t_{L>>inv}$) 0.02...10.00 s

I_L>>> Element

- I_{LCLP}>>> Activation time ($t_{LCLP>>>}$) 0.00...100.0 s
- I_L>>> Reset time delay ($t_{L>>>RES}$) 0.00...100.0 s

Definite time

- 50/51 Third threshold definite time ($I_{L>>>def}$) 0.100...40.0 I_{nL}
- $I_{L>>>def}$ within CLP ($I_{LCLP>>>def}$) 0.100...40.0 I_{nL}
- $I_{L>>>def}$ Operating time ($t_{L>>>def}$) 0.03...10.00 s

— Computed residual overcurrent - 50N/51N side H

I_{EH}> Element

- I_{EH}> Type characteristic (I_{EH}>Curve) DEFINITE
  IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, EM
- I_{EHCLP}> Activation time ($t_{ECLP>}$) 0.00...100.0 s
- I_{EH}> Reset time delay ($t_{EH>RES}$) 0.00...100.0 s

Definite time

- 50N/51N First threshold definite time ($I_{EH>def}$) 0.002...10.00 I_{nH}
- $I_{EH>def}$ within CLP ($I_{EHCLP>def}$) 0.002...10.00 I_{nH}
- $I_{EH>def}$ Operating time ($t_{EH>def}$) 0.04...200 s

Inverse time

- 50N/51N First threshold inverse time ($I_{EH>inv}$) 0.002...2.00 I_{nH}
- $I_{E>inv}$ within CLP ($I_{EHCLP>inv}$) 0.002...2.00 I_{nH}
- $I_{E>inv}$ Operating time ($t_{EH>inv}$) 0.02...60.0 s

I_{EH}>> Element

- I_{EHCLP}>> Activation time ($t_{EHCLP>>}$) 0.00...100.0 s
- I_{EH}>> Reset time delay ($t_{EH>>RES}$) 0.00...100.0 s

Definite time

- 50N/51N Second threshold inverse time ($I_{EH>>def}$) 0.002...10.00 I_{nH}
- $I_{EH>>def}$ within CLP ($I_{EHCLP>>def}$) 0.002...10.00 I_{nH}
- $I_{E>>def}$ Operating time ($t_{E>>def}$) 0.03...10.00 s

I_{EH}>>> Element

- I_{EHCLP}>>> Activation time ($t_{EHCLP>>>}$) 0.00...100.0 s
- I_{EH}>>> Reset time delay ($t_{EH>>>RES}$) 0.00...100.0 s

Definite time

- 50N/51N Third threshold definite time ($I_{EH>>>def}$) 0.002...10.00 I_{nH}
- $I_{EHCLP>>>def}$ within CLP ($I_{EHCLP>>>def}$) 0.002...10.00 I_{nH}
- $I_{EH>>>def}$ Operating time ($t_{EH>>>def}$) 0.03...10.00 s

— Computed residual overcurrent - 50N/51N side L

I_{EL}> Element

- I_{EL}> Curve type (I_{EL}>Curve) DEFINITE
  IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, EM
- I_{ELCLP}> Activation time ($t_{ECLP>}$) 0.00...100.0 s
- I_{EL}> Reset time delay ($t_{EL>RES}$) 0.00...100.0 s

Definite time

- 50N/51N First threshold definite time ($I_{EL>def}$) 0.002...10.00 I_{nL}
- $I_{EL>def}$ within CLP ($I_{ELCLP>def}$) 0.002...10.00 I_{nL}
- $I_{EL>def}$ Operating time ($t_{EL>def}$) 0.04...200 s

Inverse time

- 50N/51N First threshold inverse time ($I_{EL>inv}$) 0.002...2.00 I_{nL}
- $I_{E>inv}$ within CLP ($I_{ELCLP>inv}$) 0.002...2.00 I_{nL}
- $I_{E>inv}$ Operating time ($t_{EL>inv}$) 0.02...60.0 s

I_{EL}>> Element

- I_{ELCLP}>> Activation time ($t_{ELCLP>>}$) 0.00...100.0 s
- I_{EL}>> Reset time delay ($t_{EL>>RES}$) 0.00...100.0 s

Definite time

- 50N/51N Second threshold inverse time ($I_{EL>>def}$) 0.002...10.00 I_{nL}
- $I_{EL>>def}$ within CLP ($I_{ELCLP>>def}$) 0.002...10.00 I_{nL}
- $I_{E>>def}$ Operating time ($t_{E>>def}$) 0.03...10.00 s

I_{EL}>>> Element

- I_{ELCLP}>>> Activation time ($t_{ELCLP>>>}$) 0.00...100.0 s
- I_{ELCLP}>>> Reset time delay ($t_{EL>>>RES}$) 0.00...100.0 s

Definite time

- 50N/51N Third threshold definite time ($I_{EL>>>def}$) 0.002...10.00 I_{nL}
- ELCLP>>>$_{def}$ within CLP ($I_{ELCLP>>>def}$) 0.002...10.00 I_{nL}
- $I_{EL>>>def}$ Operating time ($t_{EL>>>def}$) 0.03...10.00 s

— Measured residual overcurrent IE1 - 50N/51N

I_{E1}> Element

- I_{E1}> Curve type (I_{E1}>Curve) INDIPENDENTE
  IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, EM
- I_{E1CLP}> Activation time ($t_{E1CLP>}$) 0.00...100.0 s
- I_{E1}> Reset time delay ($t_{E1>RES}$) 0.00...100.0 s

Definite time

- 50N/51N First threshold definite time ($I_{E1>def}$) 0.002...10.00 I_{En1}
- $I_{E1>def}$ within CLP ($I_{E1CLP>def}$) 0.002...10.00 I_{En1}
- $I_{E1>def}$ Operating time ($t_{E1>def}$) 0.04...200 s

Inverse time

- 50N/51N First threshold inverse time ($I_{E1>inv}$) 0.002...2.00 I_{En1}
- $I_{E1>inv}$ within CLP ($I_{E1CLP>inv}$) 0.002...2.00 I_{En1}
- $I_{E1>inv}$ Operating time ($t_{E1>inv}$) 0.02...60.0 s

I_{E1}>> Element
- I_{E1CLP}>> Activation time ($t_{E1CLP>>}$) 0.00...100.0 s
- I_{E1}>> Reset time delay ($t_{E1>>RES}$) 0.00...100.0 s

Definite time
- 50N/51N Second threshold inverse time ($I_{E1>>def}$) 0.002...10.00 I_{En1}
- $I_{E1>>def}$ within CLP ($I_{E1CLP>>def}$) 0.002...10.00 I_{En1}
- $I_{E1>>def}$ Operating time ($t_{E1>>def}$) 0.03...10.00 s

I_{E1}>>> Element
- I_{E1CLP}>>> Activation time ($t_{E1CLP>>>}$) 0.00...100.0 s
- I_{E1CLP}>>> Reset time delay ($t_{E1>>>RES}$) 0.00...100.0 s

Definite time
- 50N/51N Third threshold definite time ($I_{E1>>>def}$) 0.002...10.00 I_{En1}
- $I_{E1CLP>>>def}$ within CLP ($I_{E1CLP>>>def}$) 0.002...10.00 I_{En1}
- $I_{E1>>>def}$ Operating time ($t_{E1>>>def}$) 0.03...10.00 s

— Measured residual overcurrent IE2 - 50N/51N

I_{E2}> Element
- I_{E2}> Curve type (I_{E1}>Curve) INDIPENDENTE IEC/BS A, B, C, ANSI/IEEE MI, VI, EI, EM
- I_{E2CLP}> Activation time ($t_{E1CLP>}$) 0.00...100.0 s
- I_{E2}> Reset time delay ($t_{E1>RES}$) 0.00...100.0 s

Definite time
- 50N/51N First threshold definite time ($I_{E1>def}$) 0.002...10.00 I_{En2}
- $I_{E2>def}$ within CLP ($I_{E2CLP>def}$) 0.002...10.00 I_{En2}
- $I_{E2>def}$ Operating time ($t_{E2>def}$) 0.04...200 s

Inverse time
- 50N/51N First threshold inverse time ($I_{E2>inv}$) 0.002...2.00 I_{En2}
- $I_{E2>inv}$ within CLP ($I_{E2CLP>inv}$) 0.002...2.00 I_{En2}
- $I_{E2>inv}$ Operating time ($t_{E2>inv}$) 0.02...60.0 s

I_{E2}>> Element
- I_{E2CLP}>> Activation time ($t_{E2CLP>>}$) 0.00...100.0 s
- I_{E2}>> Reset time delay ($t_{E2>>RES}$) 0.00...100.0 s

Definite time
- 50N/51N Second threshold inverse time ($I_{E2>>def}$) 0.002...10.00 I_{En2}
- $I_{E2>>def}$ within CLP ($I_{E2CLP>>def}$) 0.002...10.00 I_{En2}
- $I_{E2>>def}$ Operating time ($t_{E2>>def}$) 0.03...10.00 s

I_{E2}>>> Element
- I_{E1CLP}>>> Activation time ($t_{E2CLP>>>}$) 0.00...100.0 s
- I_{E2CLP}>>> Reset time delay ($t_{E2>>>RES}$) 0.00...100.0 s

Definite time
- 50N/51N Third threshold definite time ($I_{E2>>>def}$) 0.002...10.00 I_{En2}
- $I_{E2CLP>>>def}$ within CLP ($I_{E2CLP>>>def}$) 0.002...10.00 I_{En2}
- $I_{E2>>>def}$ Operating time ($t_{E2>>>def}$) 0.03...10.00 s

— Low impedance restricted ground fault - 64REF side H
- 64REF Minimum threshold (I_{REFH}>) 0.05...2.00 I_{En1}
- 64REF Intentional delay (t_{REFH}>) 0.03...60.00 s

— Low impedance restricted ground fault - 64REF side L
- 64REF Minimum threshold (I_{REFL}>) 0.05...2.00 I_{En2}
- 64REF Intentional delay (t_{REFL}>) 0.03...60.00 s

— Differential for two windings transformer - 87T

Harmonic restraint:
- 2nd harmonic restraint (*2nd-REST*>) 10...80% I_d
- 5th harmonic restraint (*5th-REST*>) 10...80% I_d
- Restraint reset intentional delay ($t_{HREST-RES}$) 0.00...10.00 s
- Cross-harmonic restraint enabling ($C_{ROSS\ H-RES}$) ON/OFF

- *CT saturation detector*
- 87T Saturation detector enable (S_{at-Det}) ON/OFF
- 87T Saturation detector reset intentional delay ($t_{Sat-Det-RES}$) 0.00...0.50 s

- I_d> *Element Definite time*
- 87 First threshold definite time (I_d>) 0.05...2.00 I_{nref}
- 87T First stretch slope percentage (*K1*) 10...50%
- 87T Second stretch slope percentage (*K2*) 25...100%
- 87T Second stretch Intersection with vertical axis (*Q*) 0.00...3.00 I_{nref}
- 87T First threshold operating time 0.04 s

I_d>> *Element Definite time*
- 87T Second threshold definite time (I_d>>) 0.5...30.00 I_{nref}
- 87T Second threshold operating time 0.03 s

— Breaker failure - BF side H
BF Phase current threshold (I_{BFH}>) 0.05...1.00 I_{nH}
BF Residual current threshold (I_{EBFH}>) 0.01..2.00 I_{nH}
BF Time delay (t_{BFH}) 0.06...10.00 s

— Breaker failure - BF side L
BF Phase current threshold (I_{BFL}>) 0.05...1.00 I_{nL}
BF Residual current threshold (I_{EBFL}>) 0.01..2.00 I_{nL}
BF Time delay (t_{BFL}) 0.06...10.00 s

— Selective block - BLOCK2

Selective block IN:
- BLIN Max activation time for phase protections (t_{BH-Iph}) 0.10...10.00 s
- BLIN Max activation time for earth protections (t_{BH-IE}) 0.10...10.00 s

Selective block OUT:
- BLOUT Dropout time delay for phase protections (t_{FH-Iph}) 0.00...1.00 s
- BLOUT Drop-out time delay for ground protections (t_{FH-IE}) 0.00...1.00 s
- BLOUT Drop-out time delay for phase and ground protections ($t_{FH-Iph/IE}$) 0.00...1.00 s

— Internal selective block - BLOCK4
Output selective block dropout time for phase protections (t_{F-IPh}) 0.00...10.00 s
Output selective block dropout time for ground protections (t_{F-IE}) 0.00...10.00 s

— CT supervision - 74CT side H
74CT Threshold (S_H<) 0.10...0.95
74CT Overcurrent threshold (I_H*) 0.10...1.00 I_{nH}
S_H< Operate time (t_{SH}) 0.03...200 s

— CT supervision - 74CT side L
74CT Threshold (S_L<) 0.10...0.95
74CT Overcurrent threshold (I_L*) 0.10...1.00 I_{nH}
S_L< Operate time (t_{SL}) 0.03...200 s

— Circuit Breaker supervision side H
Number of CB trips (*N.Open*$_H$) 0...10000
Cumulative CB tripping currents (*SumI*$_H$) 0...5000 I_{nH}
CB opening time for I^2t calculation ΣI^2t (t_{breakH}) 0.05...1.00 s
Cumulative CB tripping I^2t (*SumI^2t*$_H$) 0...5000 $I_{nH}^2 \cdot s$
CB max allowed opening time (t_{breakH}>) 0.05...1.00 s

— Circuit Breaker supervision side L
Number of CB trips (*N.Open*$_L$) 0...10000
Cumulative CB tripping currents (*SumI*$_L$) 0...5000 I_{nL}
CB opening time for I^2t calculation ΣI^2t (t_{breakL}) 0.05...1.00 s
Cumulative CB tripping I^2t (*SumI^2t*$_L$) 0...5000 $I_{nL}^2 \cdot s$
CB max allowed opening time (t_{breakL}>) 0.05...1.00 s

— Pilot wire diagnostic
BLOUT1 Diagnostic pulses period (*PulseBLOUT1*) OFF - 0.1-1-5-10-60-120 s
BLIN1 Diagnostic pulses control time interval (*PulseBLIN1*) OFF - 0.1-1-5-10-60-120 s

METERING & RECORDING

— Measured parameters

Direct:

- Frequency f
- Fundamental RMS phase currents side H I_{L1H}, I_{L2H}, I_{L3H}
- Fundamental RMS phase currents side L I_{L1L}, I_{L2L}, I_{L3L}
- Fundamental RMS residual currents (measured) I_{E1}, I_{E2}

Calculated:

- Calculated residual current side H and L I_{EH}, I_{EL}
- Thermal image side H and L D_{ThH}, D_{ThL}
- Maximum current between I_{L1}-I_{L2}-I_{L3} side H and L I_{LmaxH}, I_{LmaxL}
- Minimum current between I_{L1}-I_{L2}-I_{L3} side H and L I_{LminH}, I_{LminL}
- Average current between I_{L1}-I_{L2}-I_{L3} side H and L I_{LH}, I_{LL}
- Compensated phase currents side H I_{L1cH}, I_{L2cH}, I_{L3cH}
- Compensated phase currents side L I_{L1cL}, I_{L2cL}, I_{L3cL}
- Stabilization currents (87 element) I_{SL1}, I_{SL2}, I_{SL3}
- Differential currents I_{dL1}, I_{dL2}, I_{dL3}
- Stabilization current (64REF-1 element) side H I_{ESH}
- Stabilization current (64REF-2 element) side L I_{ESL}

Sequence:

- Positive sequence current side H and L I_{1H}, I_{1L}
- Negative sequence current side H and L I_{2H}, I_{2L}
- Maximum of the second harmonic phase currents/fundamental component percentage ratio side H and L I_{-2nd}/I_L I_{2H}/I_{1H}, I_{2L}/I_{1L}

2nd harmonic:

- Second harmonic differential currents I_{d2L1}, I_{d2L2}, I_{d2L3}

5th harmonic:

- Fifth harmonic differential currents I_{d5L1}, I_{d5L2}, I_{d5L3}

On demand:

- Phase fixed currents demand side H I_{L1FIXH}, I_{L2FIXH}, I_{L3FIXH}
- Phase rolling currents demand side H I_{L1ROLH}, I_{L2ROLH}, I_{L3ROLH}
- Phase peak currents demand side H I_{L1MAXH}, I_{L2MAXH}, I_{L3MAXH}
- Phase minimum currents demand side H I_{L1MINH}, I_{L2MINH}, I_{L3MINH}
- Phase fixed currents demand side L I_{L1FIXL}, I_{L2FIXL}, I_{L3FIXL}
- Phase rolling currents demand side L I_{L1ROLL}, I_{L2ROLL}, I_{L3ROLL}
- Phase peak currents demand side L I_{L1MAXL}, I_{L2MAXL}, I_{L3MAXL}
- Phase minimum currents demand side L I_{L1MINL}, I_{L2MINL}, I_{L3MINL}

— Event recording (SER)

Number of events	300
Recording mode	circular

Trigger:

- Start and trip of any enabled protection or control function
- Binary inputs switching (off/on and on/off)
- Power ON and power OFF (auxiliary power supply)
- Setting changes

Data recorded:

- Event counter (resettable by ThySetter) $0...10^9$
- Event cause binary input/output relay/setting changes
- Time stamp Date and time

— Fault recording (SFR)

Number of faults	20
Recording mode	circular

Trigger:

- External trigger binary input set as Fault trigger
- Element and control pickup output relays OFF-ON transition

Data recorded:

- Time stamp Date and time
- Fault cause start, trip, binary input
- Fault counter (resettable by ThySetter) $0...10^9$
- Phase currents side H and side L I_{L1Hr}, I_{L2Hr}, I_{L3Hr}, I_{L1Lr}, I_{L2Lr}, I_{L3Lr}
- Measured residual currents I_{E1r}, I_{E2r}
- Differential currents I_{dL1r}, I_{dL2r}, I_{dL3r}
- 2nd harmonic of differential currents I_{d2L1r}, I_{d2L2r}, I_{d2L3r}
- 5th harmonic of differential currents I_{d5L1r}, I_{d5L2r}, I_{d5L3r}
- Thermal image side H and side L $D_{ThetaH-r}$, $D_{ThetaH-r}$
- Binary inputs state IN1, IN2...INx
- Output relays state K1...K6...K10
- Fault cause info (operating phase) L1, L2, L3

— Digital Fault Recorder (Oscillography)

File format	COMTRADE
Records	depending on setting [1]
Recording mode	circular
Sampling rate	16 sample/cycle

Trigger setup:

- Pre-trigger time 0.05...1.00 s
- Post-trigger time 0.05...60.00 s
- Trigger from inputs IN1, IN2...INx
- Trigger from outputs K1...K6...K10
- Communication ThySetter

Set sample channels:

- Instantaneous phase currents side H i_{L1H}, i_{L2H}, i_{L3H}
- Instantaneous phase currents side L i_{L1L}, i_{L2L}, i_{L3L}
- Compensated phase currents side H i_{L1cH}, i_{L2cH}, i_{L3cH}
- Compensated phase currents side L i_{L1cL}, i_{L2cL}, i_{L3cL}
- Stabilization currents (87 element) i_{SL1}, i_{SL2}, i_{SL3}
- Differential currents i_{dL1}, i_{dL2}, i_{dL3}
- Instantaneous measured residual currents i_{E1}, i_{E2}

Set analog channels (Analog 1...12):

- Frequency f
- Fundamental RMS phase currents side H I_{L1H}, I_{L2H}, I_{L3H}
- Fundamental RMS phase currents s side L I_{L1L}, I_{L2L}, I_{L3L}
- Thermal image side H and side L D_{ThH}, D_{ThL}
- Fundamental RMS residual currents (measured) I_{E1}, I_{E2}
- Fundamental RMS residual currents (computed) side H and L I_{EH}, I_{EL}
- Compensated phase currents side H I_{L1cH}, I_{L2cH}, I_{L3cH}
- Compensated phase currents side L I_{L1cL}, I_{L2cL}, I_{L3cL}
- Stabilization currents (87 element) I_{SL1}, I_{SL2}, I_{SL3}
- Differential currents I_{dL1}, I_{dL2}, I_{dL3}
- Second harmonic differential currents I_{d2L1}, I_{d2L2}, I_{d2L3}
- Fifth harmonic differential currents I_{d5L1}, I_{d5L2}, I_{d5L3}
- Stabilization current (64REF-1 element) side H I_{ESH}
- Stabilization current (64REF-2 element) side L I_{ESL}
- Fundamental RMS positive sequence currents side H and L I_{1H}, I_{1L}
- Fundamental RMS negative sequence currents side H and L I_{2H}, I_{2L}
- Maximum of the second harmonic phase currents/fundamental component percentage ratio side H and L I_{-2nd}/I_L I_{2H}/I_{1H}, I_{2L}/I_{1L}
- Temperature $T_1...T_8$

Set digital channels (Digital 1...12):

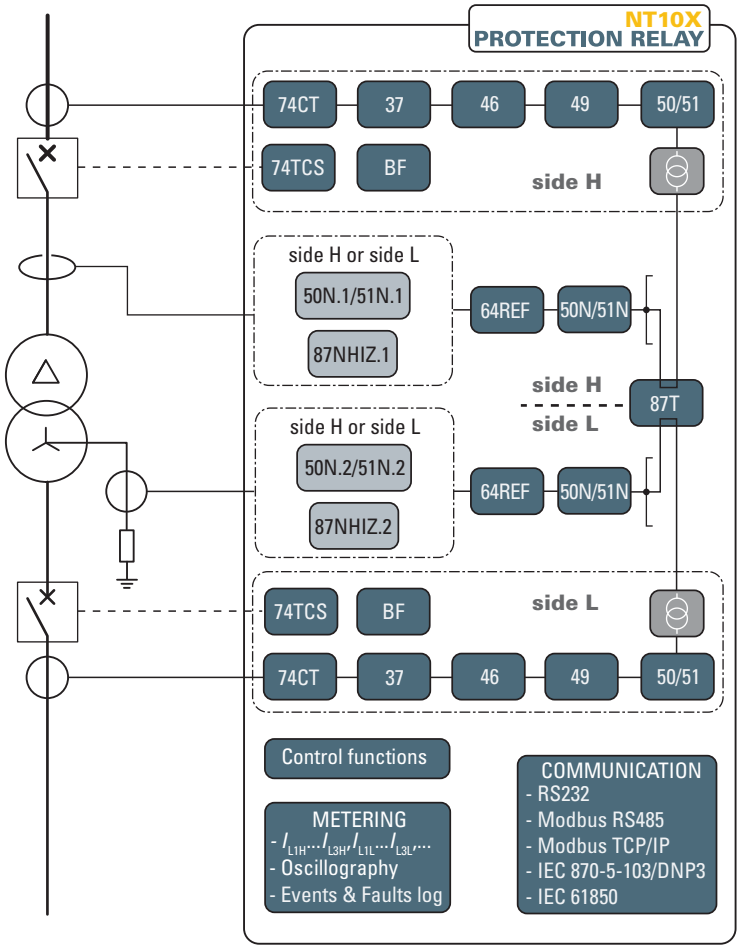
- Output relays state K1...K6...K10
- Binary inputs state IN1, IN2...INx

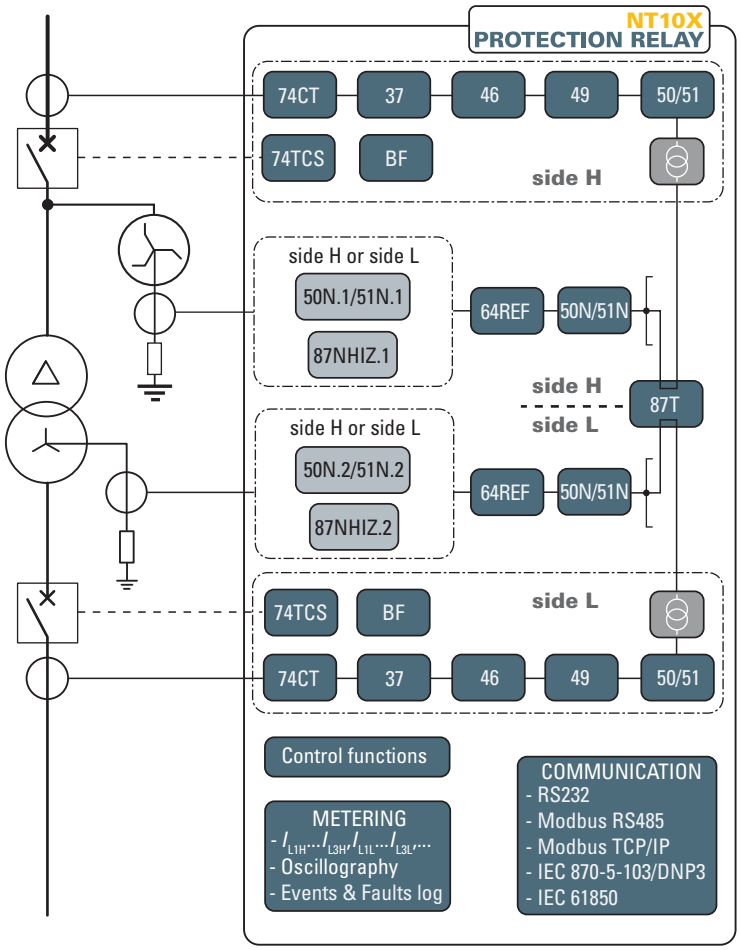
Note [1] - For instance, with following setting:

- *Pre-trigger time and Post-trigger time 0.25 s*
- *Sampled channels* i_{L1H}, i_{L2H}, i_{L3H}, i_{L1L}, i_{L2L}, i_{L3L}, i_{dL1}, i_{dL2}, i_{dL3}, i_{E1}, i_{E2}
- *Analog channels* I_{L1H}, I_{L2H}, I_{L3H}, I_{L1L}, I_{L2L}, I_{L3L}, I_{dL1}, I_{dL2}, I_{dL3}, I_{E1}, I_{E2}
- *Digital channels K1, K2, K3, K4, K5, K6, IN1, IN2*

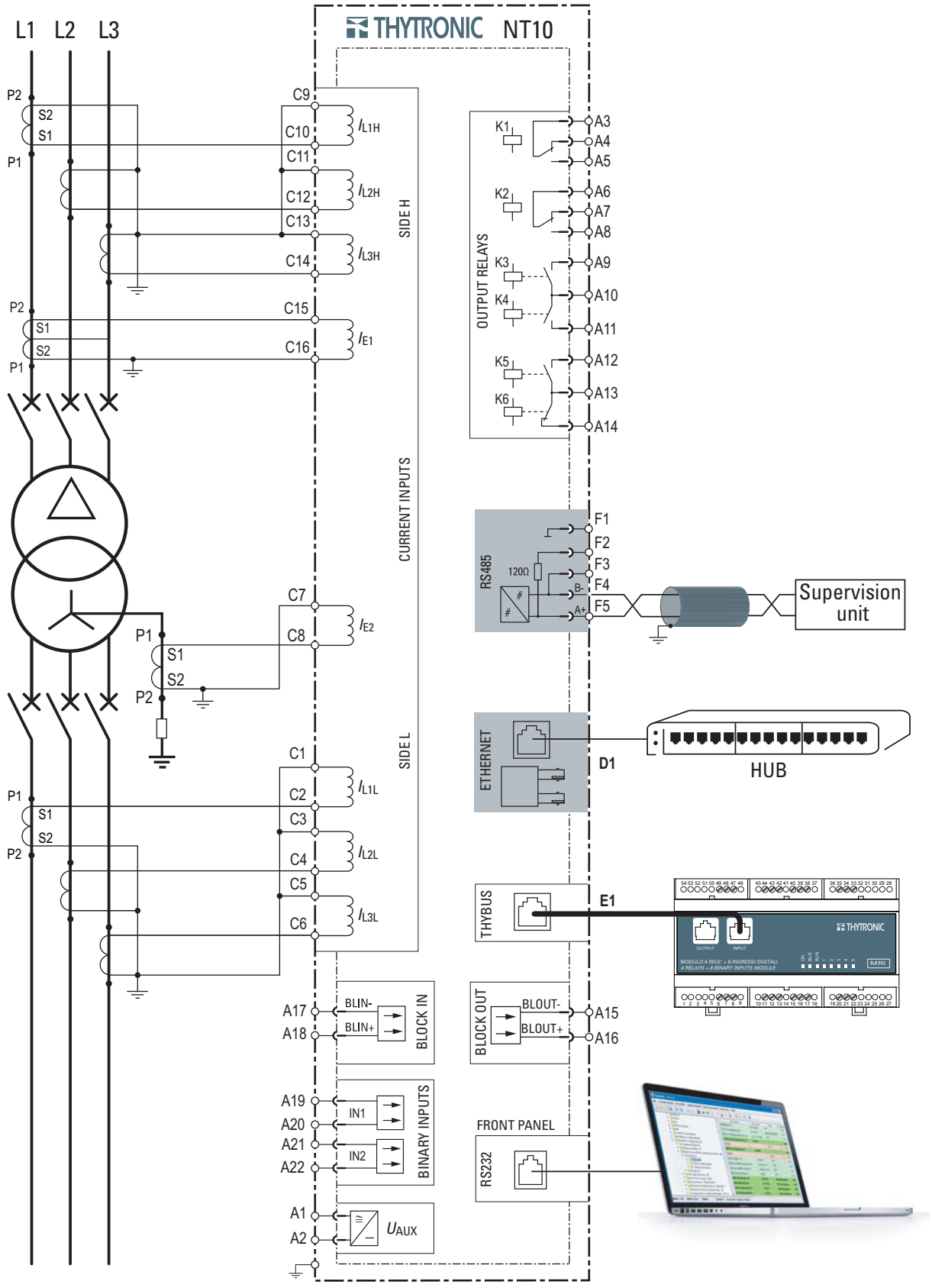
up to 200 records can be stored with f = 50 Hz

— One line diagram



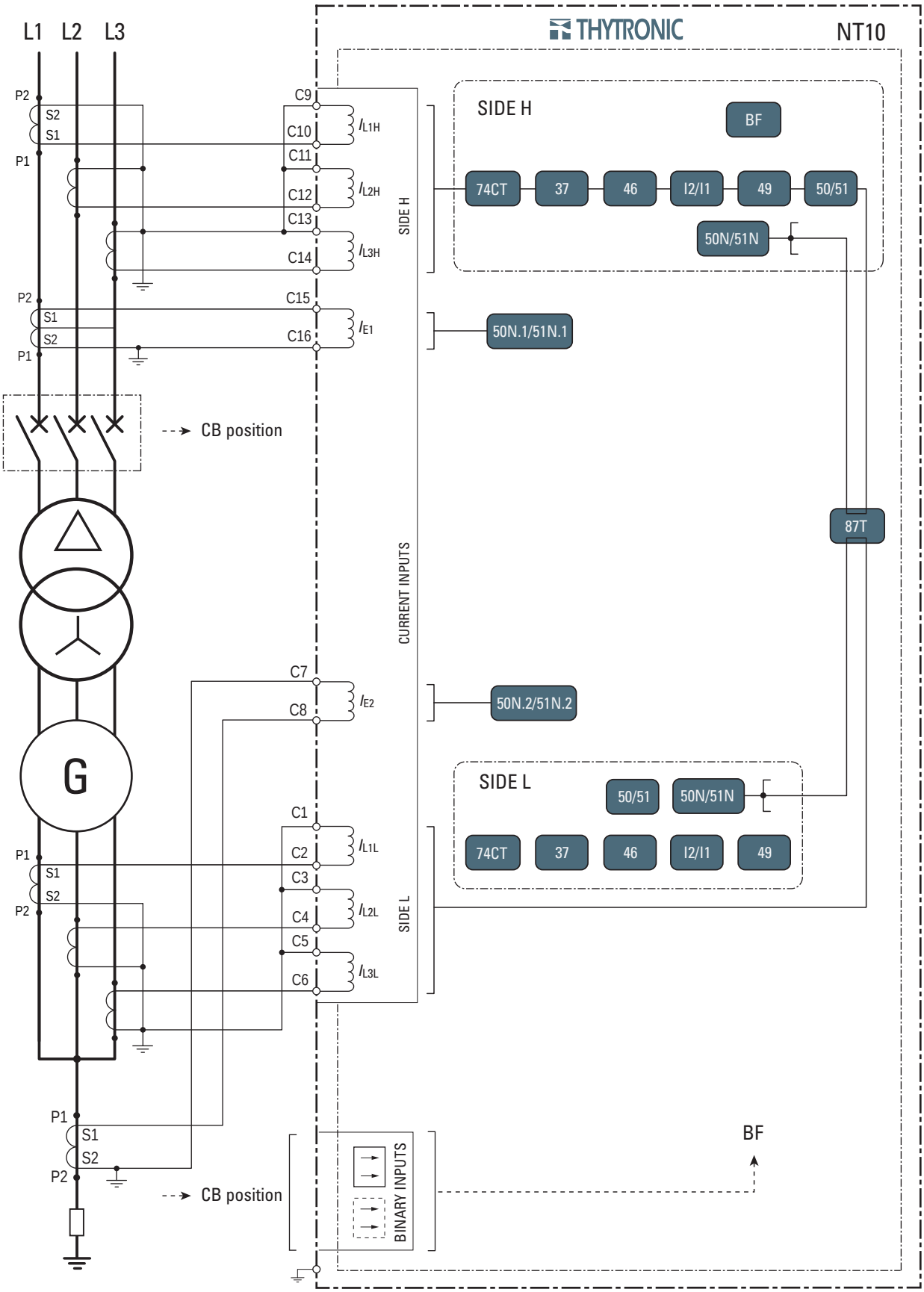


— Connection diagram example



NOTE
- Incoming currents to the protected transformer must match to the the reference current inputs of the relay, with current direction leaving the protected transformer must match current output from the current inputs of the relay.
- Incoming currents in the reference terminals of of the relay current inputs are considered positive, the outgoing negative.
- This convention applies to indicate the P1 CTs polarity toward the protected transformer.

Transformer protection - differential (87) and LV side restricted earth fault protection (64REF)

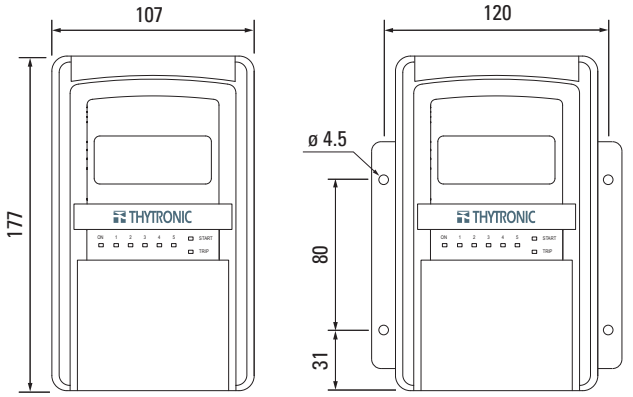


NOTE
- Incoming currents to the protected transformer must match to the the reference current inputs of the relay, with current direction leaving the protected transformer must match current output from the current inputs of the relay.
- Incoming currents in the reference terminals of of the relay current inputs are considered positive, the outgoing negative.
- This convention applies to indicate the P1 CTs polarity toward the protected transformer.

Differential protection for Transformer-Generator system

DIMENSIONS

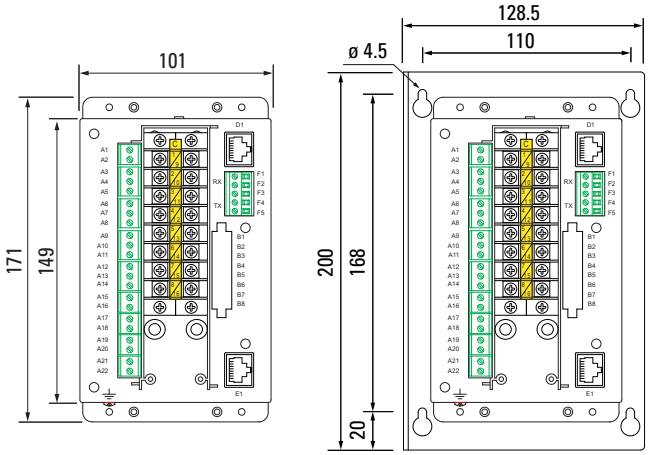
FRONT VIEW



FLUSH MOUNTING

PROJECTING MOUNTING

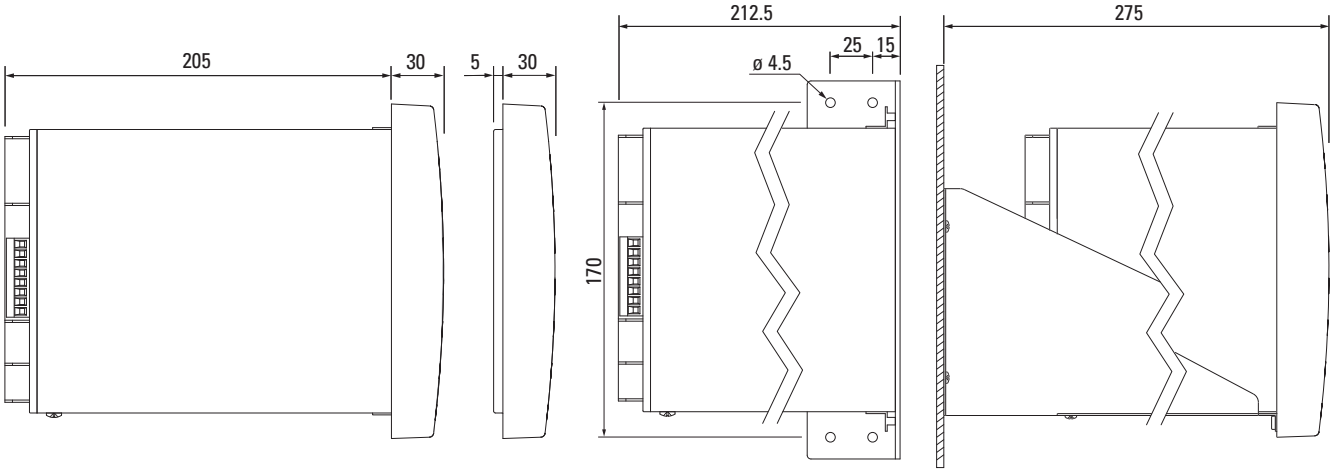
REAR VIEW



FLUSH MOUNTING

PROJECTING MOUNTING
(Separate operator panel)

SIDE VIEW



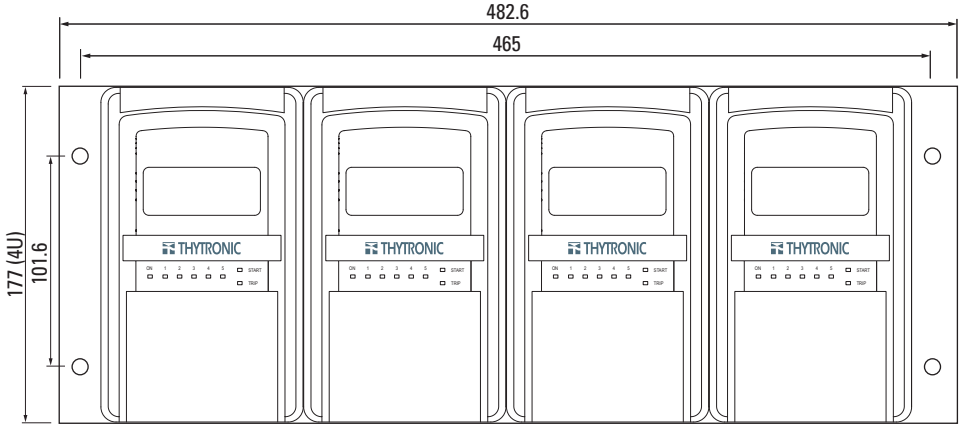
FLUSH MOUNTING

SEPARATE
OPERATOR PANEL

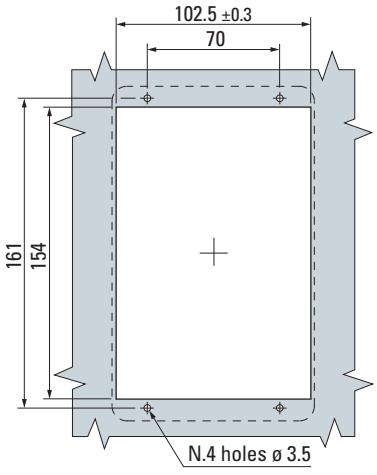
PROJECTING MOUNTING
(Separate operator panel)

PROJECTING MOUNTING
(Stand alone)

RACK MOUNTING



FLUSH MOUNTING CUTOUT



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